FIG.1

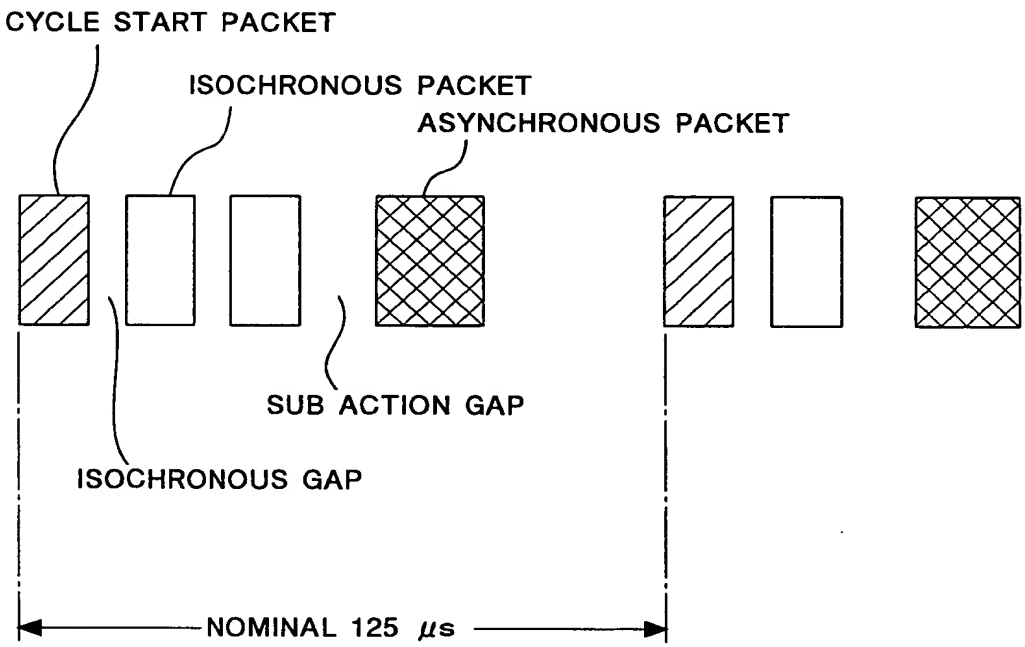

FIG.2

FIG.3

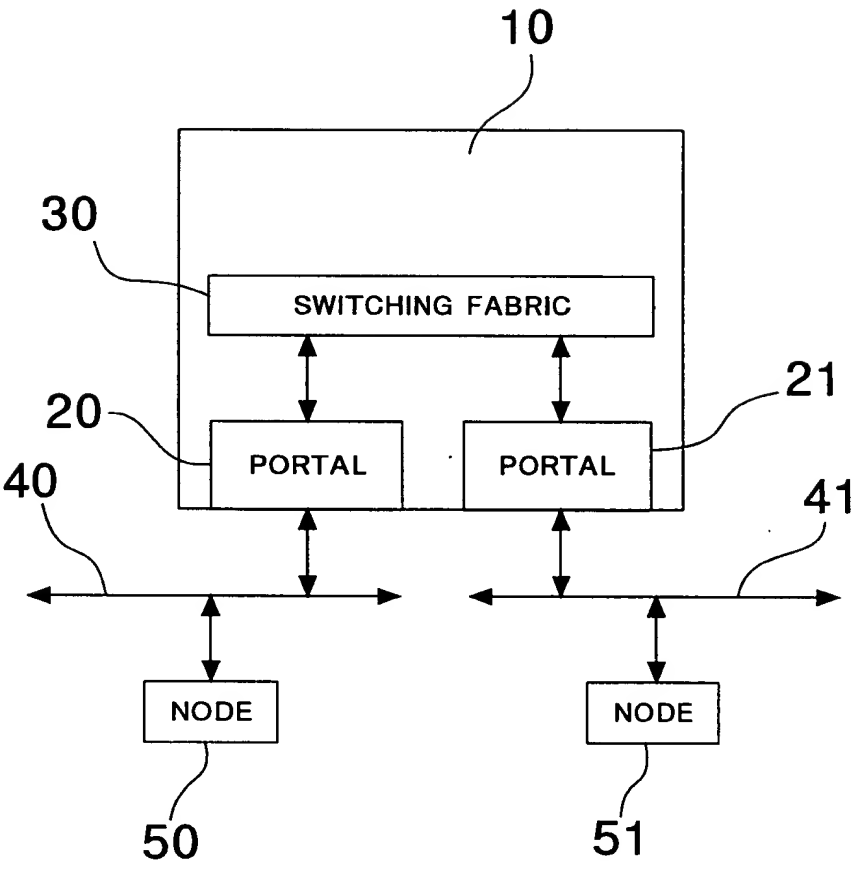

FIG.4

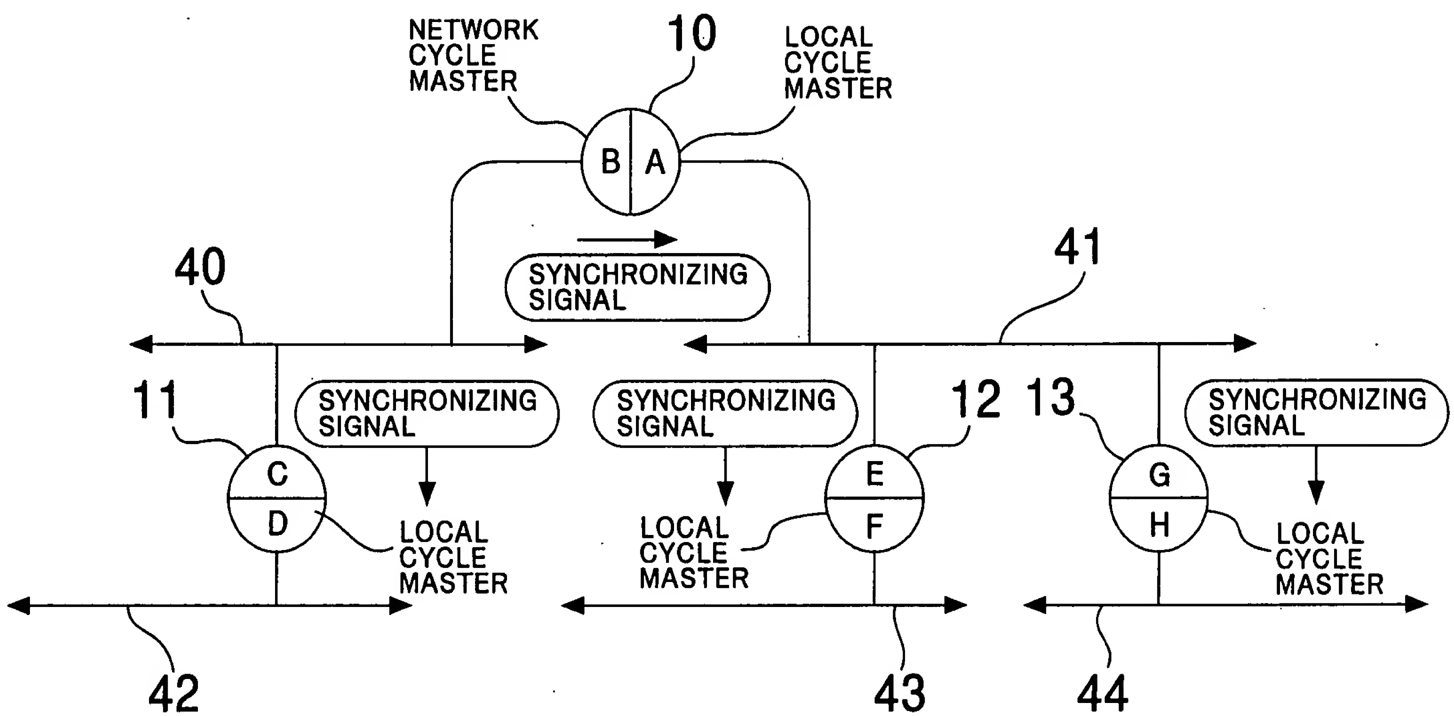
NETWORK
CYCLE
MASTER
10
LOCAL
CYCLE
MASTER
B
A
SYNCHRONIZING
SIGNAL
40
41
11
SYNCHRONIZING
SIGNAL
SYNCHRONIZING
SIGNAL
12
13
SYNCHRONIZING
SIGNAL
C
D
E
F
G
H
LOCAL
CYCLE
MASTER
LOCAL
CYCLE
MASTER
LOCAL
CYCLE
MASTER
42
43
44

FIG.5

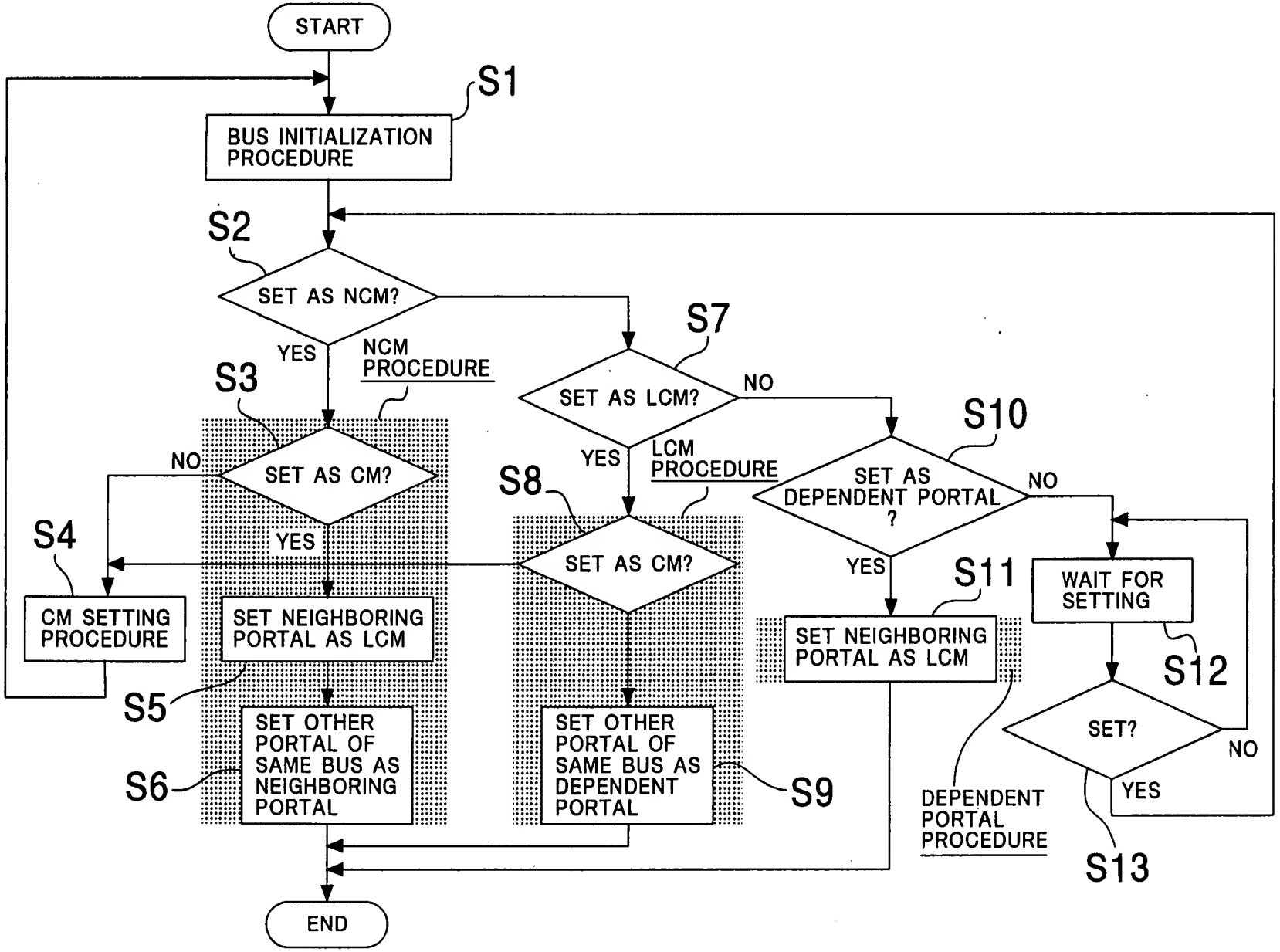

FIG.6

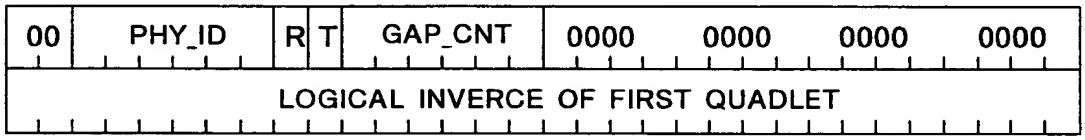

FIG.7

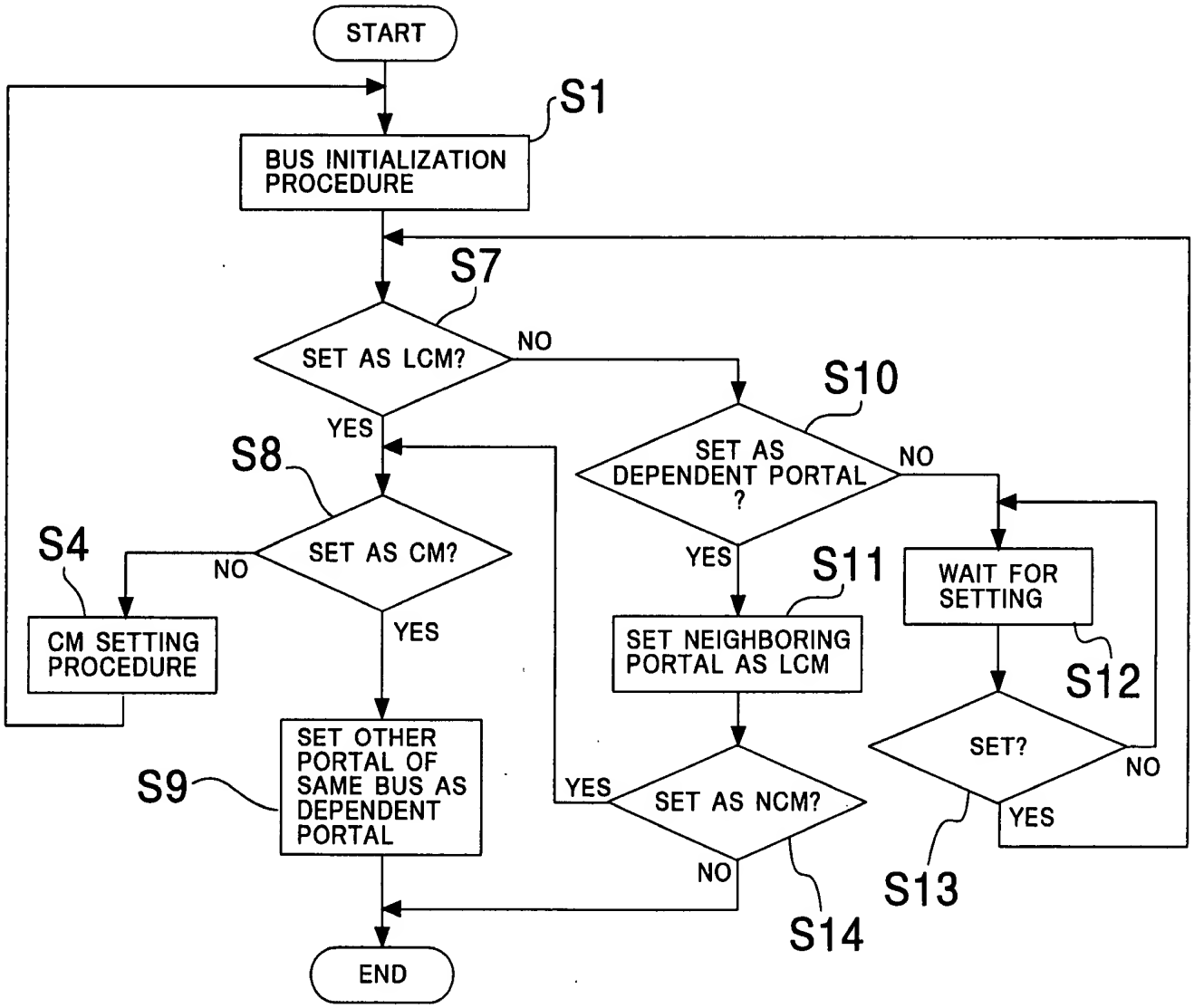

FIG.8

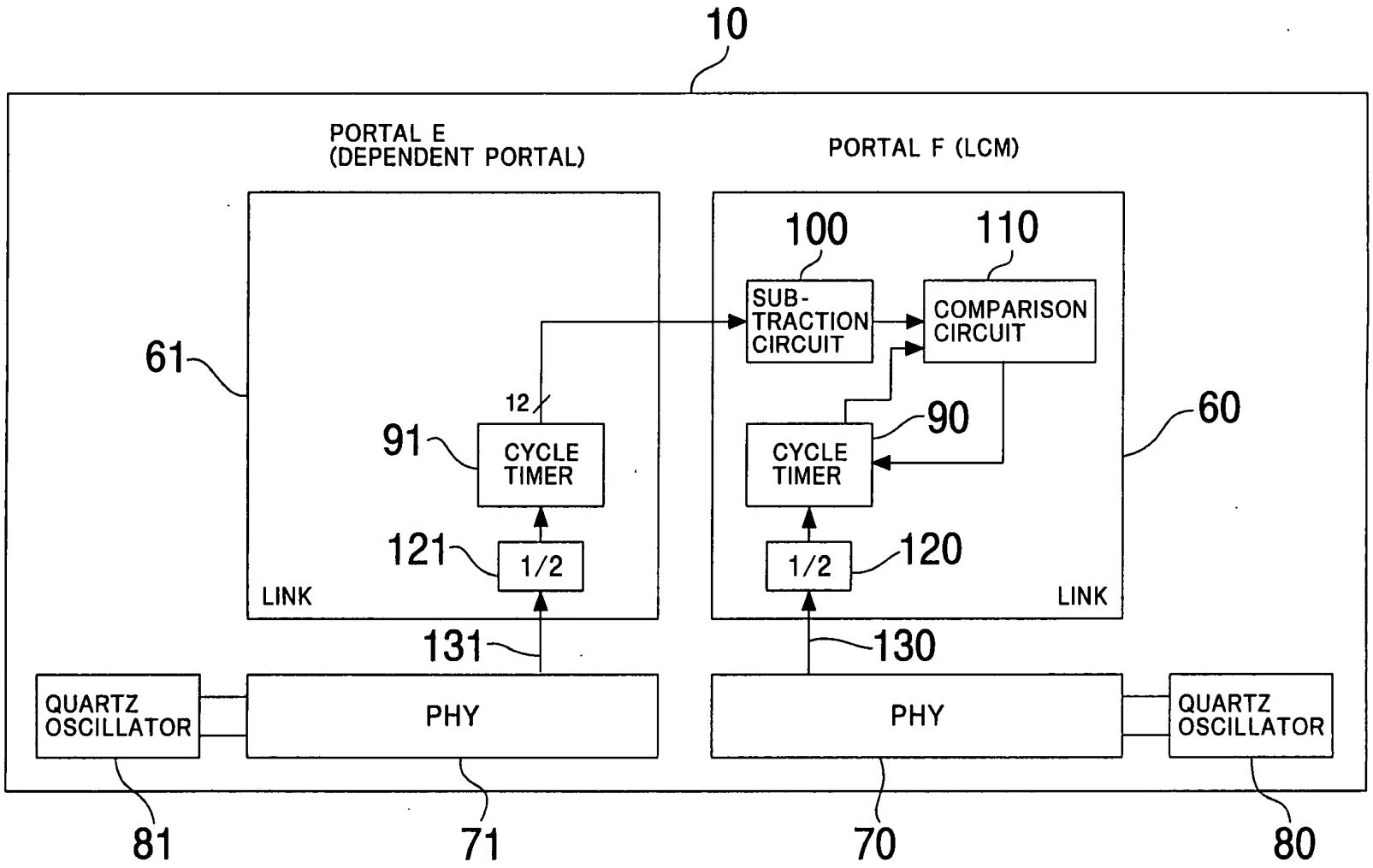
10
PORTAL E
(DEPENDENT PORTAL)
PORTAL F (LCM)
100
110
SUB-
TRACTION
CIRCUIT
COMPARISON
CIRCUIT
61
12
91
CYCLE
TIMER
90
60
CYCLE
TIMER
121
1/2
1/2
120
LINK
LINK
131
130
QUARTZ
OSCILLATOR
PHY
PHY
QUARTZ
OSCILLATOR
81
71
70
80

FIG.9

INPUT FROM SUBTRACTION CIRCUIT 100	OUTPUT OF COMPARISON CIRCUIT 110
GREATER THAN 0	01_2 (fast)
0	00_2 (stay)
SMALLER THAN 0	10_2 (slow)

FIG.10

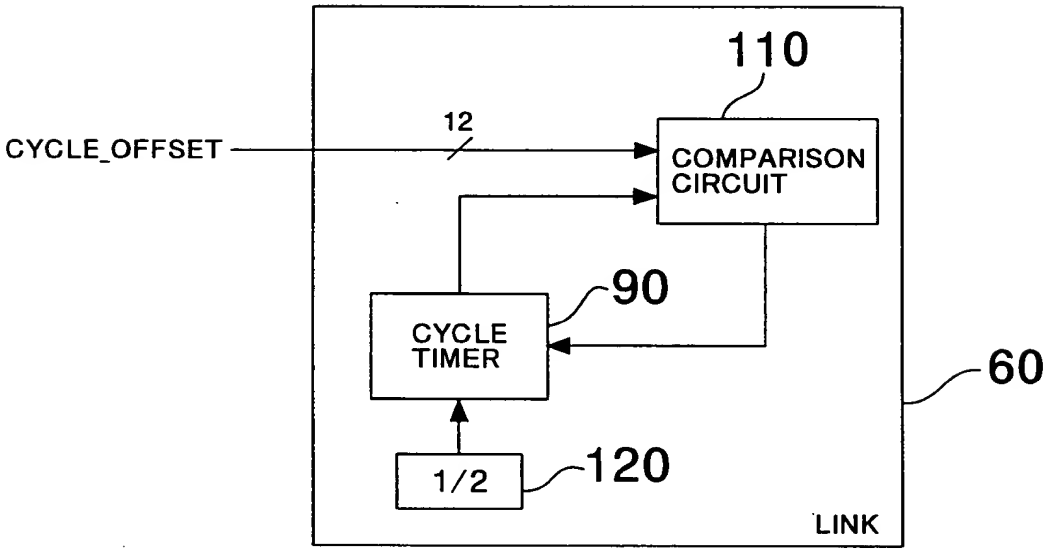

FIG.11

INPUTTED CYCLE_OFFSET	OUTPUT OF COMPARISON CIRCUIT 110
GREATER THAN 0 BUT SMALLER THAN 1,536	01_2 (fast)
0	00_2 (stay)
EQUAL TO OR GREATER THAN 1,536	10_2 (slow)

FIG.12

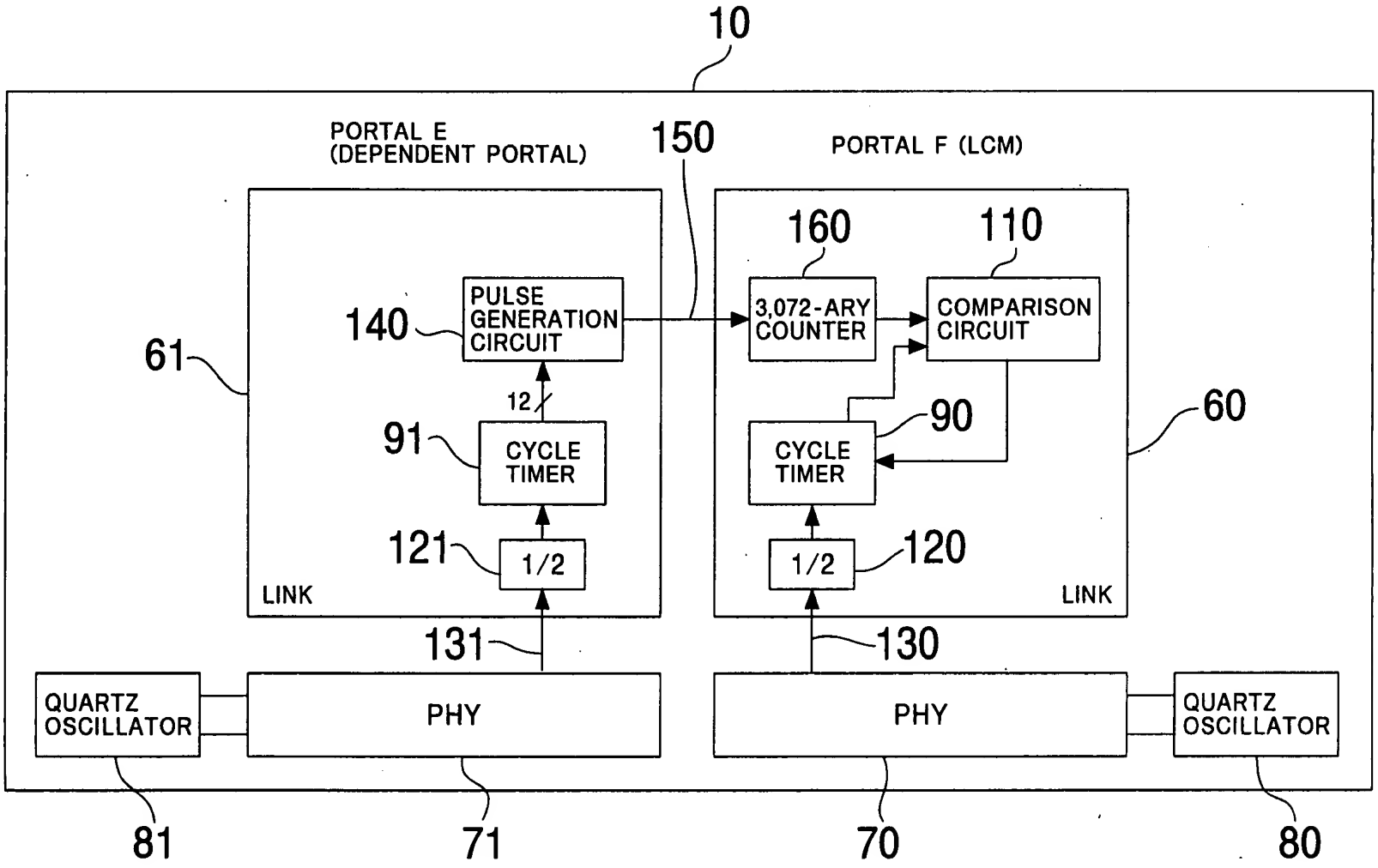

FIG.13